REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the pending application. The final Office Action dated December 28, 2004 has been received and its contents carefully reviewed.

Claims 1-13, 15-23, 27, and 32-60 are currently pending. Reexamination and reconsideration of the pending claims is respectfully requested.

Applicants appreciate the allowance of claims 13, 15-23, 33-42, and 44-60 and the indication of allowable subject matter in claims 32 and 43.

In the Office Action, the Examiner rejected claims 1-12 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Gu et al. (U.S. Pat. No. 6,359,672) in view of Shimada et al. (U.S. Patent No. 6,147,722). This rejection is respectfully traversed and reconsideration is requested.

Rejecting claim 1, the Examiner states Gu et al. teaches "that parasitic capacitance is created at overlapped areas ... and ... the relationship between the parasitic capacitance and the thickness of the layer, dielectric constant and the area of the overlap" but as failing to teach "that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line" because "the parasitic capacitance is the same between the areas of overlap of the pixel electrode with either the data line or the gate line." Attempting to cure this deficiency, the Examiner relies upon Shimada et al. as disclosing "different overlapped widths of the pixel electrodes with the gate and data lines (Fig. 3A) and (col. 12, lines 1-52)" and surmises "if one takes into consideration the different widths for the overlapped areas as taught by Shimada and calculates the parasitic capacitance... [from] the equation of Gu (col. 5, line 55), one can easily get that the parasitic capacitance in an overlapping area between the pixel electrode and the data line is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line." Applicants, however, respectfully disagree.

Specifically, the equation presented at column 5, line 55 of Gu et al. describes the relationship of parasitic capacitance with the dielectric constant of an insulation layer, the

thickness of the insulation layer, and the area of overlap between two conductors. Applicants appreciate that that an area is the product of width and length. However, Shimada et al. does not discuss the area of overlap between the pixel electrode and the data line or the area of overlap between the pixel electrode and the gate line. Moreover, Shimada et al. does not discuss the length of overlap between the pixel electrode and the data line or the length of overlap between the pixel electrode and the gate line. All that Shimada et al. discusses is the respective widths of overlap between the pixel electrode and the gate and data lines. Lacking the area of overlap or length of overlap (to supplement the disclosed width of overlap), Shimada et al. does not supply all of the information required to determine parasitic capacitance as per the equation of Gu et al. Thus, without more information (i.e., the length of overlapping areas or the actual area of the overlapping areas), Applicants respectfully submit one cannot "easily get that the parasitic capacitance in an overlapping area between the pixel electrode and the data line [of Shimada et al.] is different from a parasitic capacitance in an overlapping area between the pixel electrode and the gate line [of Shimada et al.]," as asserted by the Examiner. Because Shimada et al. lacks the requisite information necessary to determine the actual parasitic capacitances in the two areas of overlap, and because the Examiner has failed to provide any objective evidence or technical line of reasoning for asserting that the two areas of overlap discussed in Shimada et al. would be different, Applicants respectfully submit Shimada et al. fails to cure the deficiency of Gu et al. Moreover, and because the Examiner has failed to provide any objective evidence or technical line of reasoning for asserting that the two areas of overlap discussed in Shimada et al. should be different, Applicants respectfully submit that the combination of Gu et al. in view of Shimada et al. arrives at the claimed invention only with the benefit of the claimed invention, via impermissible hindsight reasoning. For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

Concluding the rejection of claim 1, the Examiner asserts it would have been obvious to "have different parasitic capacitances at the overlapped areas as taught by Shimada to achieve excellent display characteristics and high aperture ratio devices (col. 1, lines 10-12 and col. 2, liens 46-50)." Again, Applicants respectfully disagree.

Assuming *arguendo* that Shimada et al. taught different parasitic capacitances at overlapping areas of the pixel electrode and the gate and data lines, as asserted by the Examiner,

and even if the device of the device of Shimada et al. achieves excellent display characteristics and a high aperture ratio, also as asserted by the Examiner, Applicants respectfully submit such advantages are not attributable to the mere fact that the parasitic capacitance between the pixel electrode and the gate line is allegedly different from the parasitic capacitance between the pixel electrode and the data line. For example, Shimada et al. teaches that the device achieves a high aperture ratio simply because the amount by which the pixel electrode overlaps underlying conductive lines is minimized (i.e., by minimizing the enlargement of light-shading regions) (see, for example, Shimada et al. at column 13, lines 44-48; column 15, lines 25-28; column 16, lines 54-58; column 18, lines 18-21, 46-67; and column 20, lines 23-26, 63-67). Further, Shimada et al. apparently obtains "excellent display characteristics" as a result of preventing light leakage within reverse tilt domains (see, for example, Shimada et al. at column 13, lines 41-44; column 15, lines 22-25; and column 16, lines 51-54). In view of the actual teachings of Shimada et al., Applicants respectfully submit one of ordinary skill in the art would attribute the asserted advantages of Shimada et al. not to an alleged existence of different parasitic capacitances between different overlapping conductors, but to preventing light leakage within reverse tilt domains and minimizing the enlargement of light-shading regions. Because Shimada et al. fails to provide any logical connection to differences in parasitic capacitances between pixel electrodes and data lines and between pixel electrodes and gate lines with an advantageously "high aperture ratio" and "excellent display characteristics," Applicants respectfully submit that the teachings of Shimada et al. do not suggest modifying Gu et al. in a manner that obviates claim 1. For at least this additional reason, Applicants request withdrawal of the present rejection of claim 1 under 35 U.S.C. § 103(a).

In the "Response to Arguments" section of the present Office Action, the Examiner states that Shimada et al. "explicitly teaches that reverse tilt domains ... are formed with the overlap portion of the pixel electrode ... on the gate signal line ... or the source signal line ...and the excellent display characteristics is obtained by maintaining a high aperture ratio...." Nevertheless, Applicants respectfully submit Shimada et al. provides no connection between the parasitic capacitances between the two areas of overlap (i.e., between the pixel electrode and the gate signal line and between the pixel electrode and the source signal line) and the reverse tilt domains or the high aperture ratio. Accordingly, and absent evidence to the contrary, Applicants respectfully submit that the Examiner has not established different parasitic capacitances would

be reasonably expected in Gu et al. as a result of simply inserting the pixel electrode/gate and source signal line structure of Shimada et al. into Gu et al. For at least this additional reason, Applicants request withdrawal of the present rejection of claim 1 under 35 U.S.C. § 103(a).

In view of the above, Applicants respectfully submit there is no objective reason to modify Gu et al. using Shimada et al. as suggested by the Examiner. Absent any documentary evidence, technical line of reasoning, or other objective evidence, Applicants respectfully submit that the presently applied combination of Gu et al. in view of Shimada et al. arrives at claim 1 only via impermissible hindsight reasoning. For at least this additional reason, Applicants request withdrawal of the present rejection of claim 1 under 35 U.S.C. § 103(a).

Claims 2-6 and 27 depend from claim 1 and, therefore, include all of the elements recited in claim 1. As discussed above, a *prima facie* case of obviousness has not been established with respect to the elements recited in claim 1. Therefore, Applicants respectfully submit that a *prima facie* case of obviousness has not been established with respect to claims 2-6 and 27. For at least this reason, Applicants respectfully request withdrawal of the present rejection of claims 2-6 and 27 under 35 U.S.C. § 103(a).

Claim 7 was rejected using a rationale similar to that applied in the rejection of claim 1. Therefore, Applicants respectfully submit that the remarks provided above with respect to the rejection of claim 1 are equally applicable to the rejection of claim 7.

Claims 8-12 depend from claim 7 and, therefore, include all of the elements recited in claim 7. As discussed above, a *prima facie* case of obviousness has not been established with respect to the elements recited in claim 7. Therefore, Applicants respectfully submit that a *prima facie* case of obviousness has not been established with respect to claims 8-12. For at least this reason, Applicants respectfully request withdrawal of the present rejection of claims 8-12 under 35 U.S.C. § 103(a).

Applicants believe the foregoing remarks place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: March 28, 2005

Respectfully submitted,

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